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ANALYSIS OF SEQUENTIAL CIRCUITS USING LOGIC STYLES FOR LOW POWER

J. Jennifer Anne[*1] and K.Batri[2]
[*1,2]Department of ECE, PSNACET, Dindigul, India.

ABSTRACT

In an IC (Integrated Circuit) power reduction is a serious concern. There is high want for circuits which consume less power, mostly for convenient devices which run on batteries, like Laptops and hand-held computers. Reducing power consumption has a ripple effect on the rest of the system: a smaller, cheaper power supply can be used. Less power consumption means less heat, a fan may no longer be necessary; a simpler cabinet with less shielding for electromagnetic shielding may be feasible. The memory elements consume 70 percent of the total power in an IC. As flip-flops are the memory elements used in any portable devices, it is necessary to reduce the power consumption in flip-flops. It will help us to reduce the power consumption in an IC to a major extent.

Keywords- *Sequential circuits, Logic styles, Low power etc.*

I. INTRODUCTION

VLSI systems are much smaller and consume less power than the discrete components used to build electronic systems. The advantages of VLSI systems are size, cost, speed and power consumption. Thus in recent years, power consumption has become one of the major issues in electronic systems. To overcome this problem efficiently, power consumption has to be minimised. By lowering the supply voltage, the power dissipation in digital circuits is reduced.

Sequential circuits are the logic circuits whose outputs depend on both the present inputs and the past outputs. Flip flops and latches are the some of the sequential circuits which stores data. Flip flops can be either simple or clocked. The simple ones are commonly called latch and the clocked devices are described as flip flops. Sequential circuits are classified as synchronous circuits and asynchronous circuits. A simple sequential circuit is a memory cell which has two states. It can be either 1 or 0. The two state sequential circuits are called flip-flops. Flip-flops are the memory elements which are the basic building blocks of an IC.

A logic style is the method of constructing a logic gate from a set of transistors. Logic styles technique is used to reduce power in combinational circuits.

II. LITERATURE SURVEY

Different investigations of logic styles related to low power have been carried out. The D flip flop has been implemented in different CMOS logic design such as transmission gate, pass transistor logic (PTL) and gate diffusion input (GDI) logic. The design of DFF with transmission gate gives the minimum delay compared to PTL and GDI based technique and the design with pass transistor logic required minimum number of transistors. GDI based D flip flop requires minimum power of 37.56nw to design low power circuits [1]. Sequential circuits such as D flip flop, PIPO shift register and RAM are implemented in Gate diffusion input (GDI) technique which gives low power consumption, reduced delay and maintains low complexity of logic design. Gate diffusion input design style has better characteristics than CMOS, Double pass transistor and transmission gate. GDI technique can be used for low power and high performance applications [2]. Different transistor structures are used to attain better performance in terms of power. The D flip flop is designed with 18T structure and then implemented with pass transistor logic to reduce power consumption. By adding an extra NMOS in the output of the pass transistor, it further reduces the power consumption and delay of the D flip flop. The pass transistor logic style NMOS decreases power by 60% than 18T logic [3]. CMOS is considered as superior to Complementary Pass- transistor Logic in terms of speed, area, power dissipation and power-delay products. The 32-bit adder using complementary CMOS has a power-delay product of less than CPL. The Complementary CMOS performs much better than CPL. It can be used for low-power, low-voltage implementation of arbitrary combinational circuits and for design automation. Complementary Pass- transistor Logic was the efficient logic style, but Complementary CMOS proves to be superior to CPL. For simple and complex logic gates Complementary CMOS performs better. For circuit applications like multipliers CPL can be implemented for low power and high speed requirements [4]. Reducing the number of clocked transistors results in reduction of power consumption. The flip-flops designed with conventional CMOS logic consumes more power than flip-flops designed using transmission gates and pass transistors. A gated flip-flop using transmission gate and pass transistors are used to reduce the average power consumption. The D flip

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flop designed using Pass Transistor Logic dissipates lesser power [5].Five logic styles were evaluated to measure power dissipation and propagation delay. Among those static CMOS logic is the most excellent logic for speed and power dissipation characteristics. It requires 1.5V for circuit operation. In this range, the power dissipation has been reduced by one order of magnitude [6]. A reduced threshold voltage and power supply has impact on circuit design. A NAND gate is implemented in static CMOS, Differential Complementary Voltage Swing Logic (DCVSL), Domino and Pass Logic. The static CMOS logic has characteristics which are suited for many applications. Domini logic is good for high speed circuits. DCVSL is used when true and complementary functions are required [7]. A new technique is proposed based on the comparison between Conventional Transistorized Flip-flop and Data transition Look ahead D flip flop named as Pass transistor based negative edge trigged D Flip Flop(PTDFF).The D flip flop constructed using Pass Transistor Logic shows 85% improvement in power and 40% improvement in area than the normal D flip flop. This can be used in application of battery oriented function for less power and area [8]. In sequential circuits, clock overlap is the major issue. The Overlap based Logic cell is more proficient with respect to power consumption, thus the static power consumption advances in CMOS technology. Due to the usage of Overlap Period of the clock signals, the power is reduced in Overlap DFF. By using overlap based DFF the power is reduced by 35% and the number of transistors used is reduced [9]. Dual edge triggering is an efficient method for reducing the power consumption. By eliminating internal redundant transitions, they attain statistical power reduction and reduce the operating frequency by half [10]. Power consumption has a deep impact on the total power consumption. To reduce capacity of clock load, the number of clocked transistor has to be reduced. The Low swing differential capturing flip-flop (LSDCFF) consume less power and reduces capacity of clock load. The power attained from low swing differential conditional capturing flip flop is 0.298mw [11].Thus the logic styles can be used to reduce power, area and other parameters.

III. Logic Styles

A logic gate constructed from a set of transistors is called as logic style technique. Logic styles are used to reduce power and wiring complexity of a circuit. All these characteristics vary from one logic style to another.

3.1 Static logic

A static logic gate provides its output levels as long as the power supply is provided. It requires a large number of transistors to realize a function. The static CMOS logic is explained with example of 2-input NAND gate. There exists a conducting path between the output node and the ground, when input
voltages are logic high value. When one of the inputs is at low logic value, then there is a path between power supply and output node. The Fig.1 shows the 2-input NAND gate in static logic.

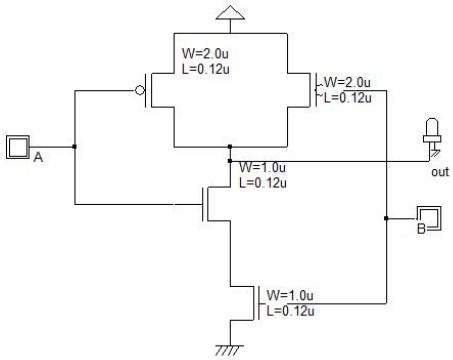

Figure.1 2-input NAND gate in Static CMOS

Characteristics of Static CMOS logic are
• Very low static power dissipation
• High noise margins
• Low output impedance and high input impedance
• No steady state path between power supply and ground
• Delay is function of load capacitance and transistor resistance
• Comparable rise and fall times

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3.2 Dynamic Logic

Dynamic logic circuits require periodic clock signals to control charge refreshing and it depends on temporary storage of charge. In this style of logic, some nodes are required to hold their
logic value as a charge stored on a capacitor. It requires reduced number of transistors to implement any logic function. In terms of propagation delay, dynamic logic styles are better. Dynamic circuits therefore require a minimum clock frequency to operate correctly.

3.3 Domino Logic

Domino logic requires a single PMOS transistor which considerably lowers the number of transistors. It reduces the input capacitance compared to CMOS. This causes increases in speed of Domino logic. The evaluation takes place faster because the logic block is constructed from only NMOS transistors. It has higher switching activity than the equivalent CMOS gate. All the output nodes are precharged to Vdd. It also dissipates large power in driving the capacitance of the clock lines. The characteristics of Domino Logic are only non-inverting logic can be implemented and it has very high speed.

3.4 Pass Transistor Logic

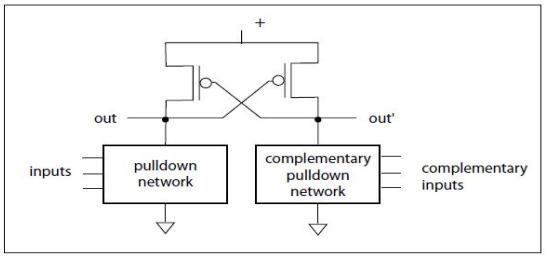
Pass Transistor Logic needs both true and complement values for input. It reduces the number of transistors by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit and thus reduce the number of active devices. The difference of the voltage between high and low logic levels decreases at each stage is the disadvantage. It can use either NMOS or PMOS to implement a function. It can be used in DRAM and SRAM.

3.5 Complementary Pass transistor Logic (CPL)

In complementary CMOS logic styles, the source side of the transistor is connected to input signals, instead of the power lines. Either PMOS or NMOS is sufficient to implement the logic function, which results in smaller number of transistors. NMOS consumes lesser power compared to PMOS. The output is “1” when logic “1” is passed through a NMOS and output is “0” when logic “0” is passed through a PMOS. Therefore, output inverters are also used.

3.6 Differential cascode voltage switch logic (DCVSL)

It is a static logic family that, like pseudo-nMOS logic, does not have a complementary pullup network, but it has a very different structure. It uses a latch structure for the pullup which both eliminates non-leakage static power consumption and provides true and complement outputs. There are two pulldown networks which are the duals of each other, one for each true/complement output. Each pulldown network has a single ptype pullup, but the pullups are cross-coupled. Exactly one of the pulldown networks will create a path to ground when the gate’s inputs change, causing the output nodes to switch to the required values. The cross-coupling of the pullups helps speed up the transition. Like CMOS static logic, there is no static power consumption. It also requires both True and Complement signals. It also provides both True and complement outputs. The circuit is self latching. This reduces ratioing requirements.



IV. CONCLUSION

The different logic styles have been studied and analysed. The structure of logic styles are analysed in different tools. By using logic styles, it reduces delay, power and increases speed of the circuit. The SCMOS gives low power. The Pass Transistor Logic requires less number of transistors. Thus the CMOS logic styles are used to reduce power consumption. Thus when sequential circuits are designed using logic styles, they consume lesser power.

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